Chapter 11

11.1. Label the wires in the circuit of Figure P11.1 as follows:

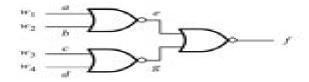


A complete fault table is

Test w ₁ w ₂ w ₃	Fault detected									
	a/0	$\alpha/1$	6/0:	$\delta \sqrt{1}$	e/0	-e/1	d/0	d/1	f/0	1/1
000								W.	W.	
001					v/		V.			V.
010					0.00		5505	V.	· V	1535
011		· v/			V		W			V
100								W.	w/	
101				· V	V		V	34.55	5,000,000	W.
110				700	- 32		1000		· •/	733
111	V		V			1		Per 50	1	

A minimal test set must include the tests $w_1w_2w_3 = 011$, 101, and 111, which cover all faults except d/1. The latter fault can be detected by choosing one of 000, 010, or 100.

11.2. Label the wires in the circuit of Figure P11.2 as follows:



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Stephen Brown, Zvonko Vranesic

<u>Fundamentals of Digital Logic with Verilog Design</u> Stephen D. Brown, Zvonko G. Vranesic, 2002 Fundamentals of Digital Logic with Verilog Design is intended for an introductory course in digital logic design which is a basic course in most Electrical and Computer Engineering programs The authors provide a desirable balance between classical and modern design approaches Basic concepts are introduced using simple logic circuits which are designed by using both manual techniques and modern CAD tool based methods Having established the fundamental concepts more complex realistic circuits are then designed with the CAD tools The Verilog language is an integral part of design techniques used throughout the book Altera's advanced Max plus II CAD systmem on CD ROM and a series of step by step tutorials are included

Fundamentals of Digital Logic with Verilog Design Stephen Brown, Zvonko Vranesic, 2013-03-15 Fundamentals of Digital Logic With Verilog Designteaches the basic design techniques for logic circuits It emphasizes the synthesis of circuits and explains how circuits are implemented in real chips Fundamental concepts are illustrated by using small examples Use of CAD software is well integrated into the book A CD ROM that contains Altera's Quartus CAD software comes free with every copy of the text The CAD software provides automatic mapping of a design written in Verilog into Field Programmable Gate Arrays FPGAs and Complex Programmable Logic Devices CPLDs Students will be able to try firsthand the book s Verilog examples over 140 and homework problems Engineers use Quartus CAD for designing simulating testing and implementing logic circuits. The version included with this text supports all major features of the commercial product and comes with a compiler for the IEEE standard Verilog language Students will be able to enter a design into the CAD system compile the design into a selected device simulate the functionality and timing of the resulting circuit implement the designs in actual devices using the school's laboratory facilities Verilog is a complex language so it is introduced gradually in the book Each Verilog feature is presented as it becomes pertinent for the circuits being discussed To teach the student to use the Quartus CAD the book includes three tutorials Instructor's Solutions Manual to Accompany Fundamentals of Digital Logic with Vhdl Design Lord Brown, Stephen D. Brown, Zvonko G. Vranesic, 1999-10-01 Embedded SoPC Design with Nios II Processor and Verilog Examples Pong P. Chu, 2012-05-14 Explores the unique hardware programmability of FPGA based embedded systems using a learn by doing approach to introduce the concepts and techniques for embedded SoPC design with Verilog An SoPC system on a programmable chip integrates a processor memory modules I O peripherals and custom hardware accelerators into a single FPGA field programmable gate array device In addition to the customized software customized hardware can be developed and incorporated into the embedded system as well allowing us to configure the soft core processor create tailored I O interfaces and develop specialized hardware accelerators for computation intensive tasks Utilizing an Altera FPGA prototyping board and its Nios II soft core processor Embedded SoPC Design with Nios II Processor and Verilog Examples takes a learn by doing approach to illustrate the hardware and software design and development

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