## Cryptographic Hardware & Embedded Systems for Communications

Nicolas Sklavos, Member, IEEE, Invited Speaker

Abstract— This work is related to System-On-A-Chip architectures and design methodologies, for cryptographic algorithms implementations. Alternative approaches are presented, for architecture and architectures for block ciphers, stream ciphers, and hash functions. The presented algorithms are the most wide used, in all certain of modern applications. Implementation aspects are given for both ASIC and FPGA integration platforms. Synthesis results are illustrated in hardware terms. This work also introduces the basic principles of random number generators, which are fundamental primitives of security applications also. Comparisons of operating frequency, throughput and allocated resources are given in detail. Future directions in hardware and embedded systems design, concerning Ardulno platforms and open source programming, are also given.

Index Terms— security, cryptography, computer architecture, system-on-a-chip, FPGA, ASIC, VLSI design, embedded systems, Arduino

#### I. INTRODUCTION

THE spreading revolution of communications, and especially the wireless and mobile applications of them, has created special needs for safe and secure communications [1]. With the adoption of the hardware advantages the center of interest has been moved to cryptographic hardware, regarding implementation aspects, of security primitives [2]. With the term cryptographic hardware, the research community refers to both theoritical and practical adoptions of cryptographic engineering, for a variety of purposes and applications such as: encryption and decryption processors, digital signature systems, key generation and distribution schemes, as well as random number generators [3]. In order to implement efficiently a security system, first the responsible team has to design, to implement, to validate and to test the implementation for the efficient performance of it [2].

This work introduces the aspects of cryptographic hardware and embedded systems, regarding implementation issues, for several aspects of secure communications: block ciphers, hash functions, random number generators, etc. It is also presented future directions, concerning promising hardware devices such as Arduino, and gives aspects of open source programming of them.

Nicolas Sklavos is with the KNOSSOSnet Research Group, Informatics & MM Department, Technological Educational Institute of Patras, Hellas, (email: mklavos@iopc.org).

#### II. DESIGN PROCESS: SYSTEM-ON-A-CHIP

This paragraph is related to the basics of System-On-A-Chip design process, which contains the following sections: SoC design, design flow and design life through specifications [4-6].

#### A. SoC Design

Let's assume the design of a crypto-processor for a specific purpose like secure satellite communications, which is illustrated in the next Figure 1:

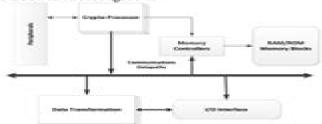


Fig. 1. Crypto-Processor Architecture of a Canonical SoC Design

The main subsystems are: the crypto-processor, the memories sub-blocks (RAM/ROM, memory controllers). I/O interfaces with the external communication systems, units data transformation units, as well as communication datapaths [4]. Such a design, although maybe seemed generic, applies most of the structures and methodologies, that are used in SoC design [5]. The internal subsystems vary in nature and in performance issues. These blocks will be design developed and specified, during the design process. According to the application needs its time, the above design could be transformed to a more complicated one, which may integrates different interfaces, data transformations, a set of different processors, as well as a number of other peripherals and subsystems like memory units [4].

#### B. Design Flow

In most of the cases, designers do achieve to meet the requirements of the application design, through two alternative design flows. Regarding ASICs (Application Specific Integrated Circuits), the waterfall model is followed. Fig. 2. According to this model, the design process is divided to seven alternative stages, which can be implemented by

Emmanuel Prouff, Patrick R. Schaumont

Embedded Cryptographic Hardware Nadia Nedjah, Luiza de Macedo Mourelle, 2005 Data security is an important requirement for almost all if not all information oriented applications such as e commerce digital signature secure Internet etc All these services use encrypted data Cryptography is a milliner science that was the key to the secret of ancient Rome and a fundamental piece in the Second World War Today it is a star in the computation world Several operating systems data base systems or simple filling systems provide the user with cryptographic functions that allow controlled data scrambling Modern cryptology which is the basis of information security techniques started in the late 1970 s and developed in the 1980 s As communication networks were spreading deep into society the need for secure communication greatly promoted cryptographic research The need for fast but secure cryptographic systems is growing bigger Therefore dedicated hardware for cryptography is becoming a key issue for designers With the spread of reconfigurable hardware such as FPGAs hardware implementations of cryptographic algorithms became cost effective. The focus of this book is on all aspects of cryptographic hardware and embedded systems This includes design implementation and security of such systems The content of this book is divided into four main parts each of which is organised in three chapters with the exception of the last one Cryptographic Hardware Nadia Nedjah, Luiza de Macedo Mourelle, 2004 Modern cryptology which is the basis of information security techniques started in the late 70 s and developed in the 80 s As communication networks were spreading deep into society the need for secure communication greatly promoted cryptographic research The need for fast but secure cryptographic systems is growing bigger Therefore dedicated systems for cryptography are becoming a key issue for designers With the spread of reconfigurable hardware such as FPGAs hardware implementations of cryptographic algorithms become cost effective The focus of this book is on all aspects of embedded cryptographic hardware Of special interest are contributions that describe new secure and fast hardware implementations and new efficient algorithms methodologies and protocols for secure communications This book is organised in two parts The first part is dedicated to embedded hardware of cryptosystems while the second part focuses on new algorithms for cryptography design methodologies and secure protocols

held in Washington D C USA during August 10 13 2008 The book contains 2 invited talks and 27 revised full papers which were carefully reviewed and selected from 107 submissions The papers are organized in topical sections on side channel analysis implementations fault analysis random number generation and cryptography and cryptanalysis Hardware and Embedded Systems ,1999 **Cryptographic Hardware and Embedded Systems -- CHES 2012** Emmanuel Prouff, Patrick R. Schaumont, 2012-09-05 This book constitutes the proceedings of the 14th International Workshop on Cryptographic Hardware and Embedded Systems CHES 2012 held in Leuven Belgium in September 2012 The 32 papers presented together with 1 invited talk were carefully reviewed and selected from 120 submissions. The papers are organized in the following topical sections intrusive attacks and countermeasures masking improved fault attacks and side channel analysis leakage resiliency and security analysis physically unclonable functions efficient implementations lightweight cryptography we still love RSA and hardware implementations Cryptographic Hardware and Embedded Systems -- CHES 2015 Tim Güneysu, Helena Handschuh, 2015-08-31 This book constitutes the refereed proceedings of the 17th International Workshop on Cryptographic Hardware and Embedded Systems CHES 2015 held in Saint Malo France in September 2015 The 34 full papers included in this volume were carefully reviewed and selected from 128 submissions. They are organized in the following topical sections processing techniques in side channel analysis cryptographic hardware implementations homomorphic encryption in hardware side channel attacks on public key cryptography cipher design and cryptanalysis true random number generators and entropy estimations side channel analysis and fault injection attacks higher order side channel attacks physically unclonable functions and hardware trojans side channel attacks in practice and lattice based implementations Embedded Cryptographic Hardware Nadia Nedjah, Luiza de Macedo Mourelle, 2004 Modern cryptology which is the basis of information security techniques started in the late 70 s and developed in the 80 s As communication networks were spreading deep into society the need for secure communication greatly promoted cryptographic research The need for fast but secure cryptographic systems is growing bigger Therefore dedicated systems for cryptography are becoming a key issue for designers With the spread of reconfigurable hardware such as FPGAs hardware implementations of cryptographic algorithms become cost effective. The focus of this book is on all aspects of embedded cryptographic hardware Of special interest are contributions that describe new secure and fast hardware implementations and new efficient algorithms methodologies and protocols for secure communications This book is organised in two parts The first part is dedicated to embedded hardware of cryptosystems while the second part focuses on new algorithms for cryptography design methodologies and secure protocols Cryptographic Hardware and Embedded Systems -- CHES 2010 Stefan Mangard, Francois-Xavier Standaert, 2010-08-08 Annotation This book constitutes the refereed proceedings of the 12th International Workshop on Cryptographic Hardware and Embedded Systems CHES 2010 held in Santa Barbara USA during August 17 20 2010 This year it was co located with the 30th International Cryptology

Conference CRYPTO The book contains 2 invited talks and 30 revised full papers which were carefully reviewed and selected from from 108 submissions. The papers are organized in topical sections on low cost cryptography efficient implementation side channel attacks and countermeasures tamper resistance hardware trojans PUFs and RNGs **Cryptographic** Hardware and Embedded Systems - CHES 2001 Cetin K. Koc, David Nacchae, Christof Paar, 2003-06-30 These are the proceedings of CHES 2001 the third Workshop on Cryptographic Hardware and Embedded Systems The rst two CHES Workshops were held in Massachusetts and this was the rst Workshop to be held in Europe There was a large number of submissions this year and in response the technical program was extended to 2 1 2 days As is evident by the papers in these proceedings many excellent submissions were made Selecting the papers for this year's CHES was not an easy task and weregretthatwehadtorejectseveralveryinterstingpapersduetotheac l kof time There were 66 submitted contributions this year of which 31 or 47% were selected for presentation If we look at the number of submitted papers at CHES 99 42 papers and CHES 2001 51 papers we observe a steady increase We interpret this as a continuing need for a workshop series which combines theory and practice for integrating strong security features into modern communications and computer applications In addition to the submitted contributions Ross Anderson from Cambridge University UK and Adi Shamir from The Weizmann Institute Israel gave invited talks As in previous years the focus of the workshop is on all aspects of cryp graphichardwareandembeddedsystemdesign Ofspecialinterestwerecont butions that describe new methods for e cient hardware implementations and high speed software for embedded systems e g smart cards microprocessors DSPs etc CHES also continues to be an important forum for new theoretical and practical ndings in the important and growing eldofside channelattacks Cryptographic Hardware and Embedded Systems - CHES 2004 Marc Jove, Jean-Jagues Quisquater, 2004-07-08 These are the proceedings of CHES 2004 the 6th Workshop on Cryptographic Hardware and Embedded Systems For the first time the CHES Workshop was sponsored by the International Association for Cryptologic Research IACR This year the number of submissions reached a new record One hundred and twenty five papers were submitted of which 32 were selected for presentation Each submitted paper was reviewed by at least 3 members of the program committee We are very grateful to the program committee for their hard and efficient work in assembling the program We are also grateful to the 108 external referees who helped in the review process in their area of expertise In addition to the submitted contributions the program included three invited talks by Neil Gershenfeld Center for Bits and Atoms MIT about Physical Information Security by Isaac Chuang Medialab MIT about Quantum Cryptography and by Paul Kocher Cryptography Research about Phy cal Attacks It also included a rump session chaired by Christof Paar which featured informal talks on recent results As in the previous years the workshop focused on all aspects of cryptographic hardware and embedded system security We sincerely hope that the CHES Workshop series will remain a premium forum for intellectual exchange in this area Cryptographic Hardware and Embedded Systems - CHES 2016 Benedikt Gierlichs, Axel Y.

Poschmann,2016-08-03 This book constitutes the proceedings of the 18th International Conference on Cryptographic Hardware and Embedded Systems CHES 2016 held in Santa Barbara CA USA in August 2016 The 30 full papers presented in this volume were carefully reviewed and selected from 148 submissions They were organized in topical sections named side channel analysis automotive security invasive attacks side channel countermeasures new directions software implementations cache attacks physical unclonable functions hardware implementations and fault attacks

Cryptographic Hardware and Embedded Systems - CHES 2002 Burton S. Jr. Kaliski, Cetin K. Koc, Christof Paar, 2003-08-02 These are the proceedings of CHES 2002 the Fourth Workshop on Cryptographic Hardware and Embedded Systems After the rst two CHES Workshops held in Massachusetts and the third held in Europe this is the rst Workshop on the West Coast of the United States There was a record number of submissions this year and in response the technical program was extended to 3 days As is evident by the papers in these proceedings there have been again many excellent submissions Selecting the papers for this year's CHES was not an easy task and we regret that we could not accept many contributions due to the limited availability of time There were 101 submissions this year of which 39 were selected for presentation We continue to observe a steady increase over previous years 42 submissions at CHES 99 51 at CHES 2000 and 66 at CHES 2001 We interpret this as a continuing need for a workshop series that c bines theory and practice for integrating strong security features into modern communications and computer applications. In addition to the submitted cont butions Jean Jacques Quisquater UCL Belgium Sanjay Sarma MIT USA and a panel of experts on hardware random number generation gave invited talks As in the previous years the focus of the Workshop is on all aspects of cr tographic hardware and embedded system security Of special interest were c tributionsthatdescribenewmethodsfore cienthardwareimplementations and high speed software for embedded systems e q smart cards microprocessors DSPs etc CHES also continues to be an important forum for new theoretical and practical ndings in the important and growing eld of side channel attacks Cryptographic Hardware and Embedded Systems - CHES 2009 Christophe Clavier, Kris Gaj, 2009-08-28 CHES 2009 the 11th workshop on Cryptographic Hardware and Embedded Systems was held in Lausanne Switzerland September 6 9 2009 The wo shop was sponsored by the International Association for Cryptologic Research IACR The workshop attracted a record number of 148 submissions from 29 co tries of which the Program Committee selected 29 for publication in the wo shop proceedings resulting in an acceptance rate of 19 6% the lowest in the history of CHES The review process followed strict standards each paper ceived at least four reviews and some asmanyaseightreviews Membersofthe Program Committee were restricted to co authoring at most two submissions and their papers were evaluated by an extended number of reviewers The ProgramCommittee included 53 members representing 20 countries and ve continents These members were carefully selected to represent academia industry and government as well as to include world class experts in various research elds of interest to CHES The Program Committee was supported by 148 external

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